Intel® High Definition Audio Specification
Document Change Notification

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Document Revision:	Intel® High Definition Audio 1.0

Title: Clarification of DMA Position Lower Base Address

Brief description of the functional changes:

The definition in the HD Audio specification provides a 32 bit register for the lower base address of the DMA Position Base Address. The lower 7 bits of this register are alternately defined but with no clarity on bits 31:7 being the only valid bits and bits 6:0 not part of that 32 bit address. This ECR clarifies that bits 31:7 are the top portion of the lower base address and correspond to bits 31:7 of the DMA Position Lower Base Address and that the bottom 7 bits of the DMA Position Base Address are always 0.

Current Definitions:

3.3.32 Offset 70h: DPLBASE – DMA Position Lower Base Address

Length: 4 bytes

Table 1. DMA Position Lower Base Address

Bit	Type	Reset	Description
31:7	RW	0's	**DMA Position Lower Base Address (DPLBASE):** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	RO	0's	**DMA Position Lower Base Unimplemented Bits:** Hardwired to 0 to force 128-byte buffer alignment for cache line write optimizations.
0	RW	0	**DMA Position Buffer Enable:** When this bit is set to a 1, the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically. Software can use this value to know what data in memory is valid data. The controller must ensure that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer; the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

New Definition:

3.3.32 Offset 70h: DPLBASE – DMA Position Lower Base Address

Length: 4 bytes

Table 2. DMA Position Lower Base Address

Bit	Type	Reset	Description
31:7	RW	0's	**DMA Position Lower Base Address (DPLBASE):** Contains the upper 25 bits of the lower 32 bits of the DMA Position Buffer Base Address. The lower 7 bits of the DMA Position Buffer Base Address are always zero and not programmable to allow for 128 byte alignment and cache line write optimizations. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	RsvdZ	0's	*Reserved*
0	RW	0	**DMA Position Buffer Enable:** When this bit is set to a 1, the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically. Software can use this value to know what data in memory is valid data. The controller must ensure that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer; the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.